



LUMI ETC Review

Introduction & FY08 Summary

Alex



Agenda

8:00 - Executive session 15'

08:15 Alex Ratti - Project Status (35' + 10')

09:00 Howard Matis – Physics Modeling and Beam Studies (20' + 5')

09:25 Break

09:45 Alex Ratti – Scope to Complete (50' +10')

10:45 Howard Matis – Beam Commissioning Plans (20' + 5')

11:10 Alex Ratti & Sergio Zimmermann – Budget and Schedule (20' + 5')

11:35 Discussion



Introduction

- Having to execute a project within a program, we cover **two** separate and nearly independent plans
 - Lumi Construction Project
 - Lumi System Commissioning with Beam
- Review the plan to complete luminosity monitors production and installation
- Present plans for detector development and operation during beam commissioning



Outline

- History
- Status at CERN
- Production and testing highlights
- Path to completion (LATER TALK)

Most of my talks will cover the lumi
construction project



Accomplishments in FY08

- Recorded first beam on day one
- Delivered four detectors to CERN
- Completed (simplified) gas systems
- Completed phase 1 firmware and software programming
- Systems integration underway



FY08 Highlights

- HV cables performance
 - Initial design had unexpected leaks
 - Caused noise comparable to actual lumi signals
 - Resulted in the complete redesign of the flange/HV cable assembly



FY08 Highlights (cont.)

- Recovered from HV cable leaks
 - Now working on integration of PA and Detector
- As we were developing a solution for HV cables, we completed the detectors
 - Two shipped and installed in LHC in Spring
 - Adequate for low luminosity run in 2008
 - Must be retrofit to match final design
 - Balance (2 more) at CERN ready for installation
 - New configuration completed in September



Cost Control Measures

- Descoping
 - Gas system
 - Online radiation damage monitoring
- Delayed
 - Shaper Integration
 - Pre-Amp Production



CERN's Position

- Bravin's memo - June 1
 - CERN procured and installed a PMT based system for 2008 run
 - LBNL/LARP should focus on making sure ionization chambers are ready in 2009
 - Devices have to be installed and commissioned by day one of the 2009 run
 - CERN will monitor very closely
 - Control systems support limited by beam commissioning priority

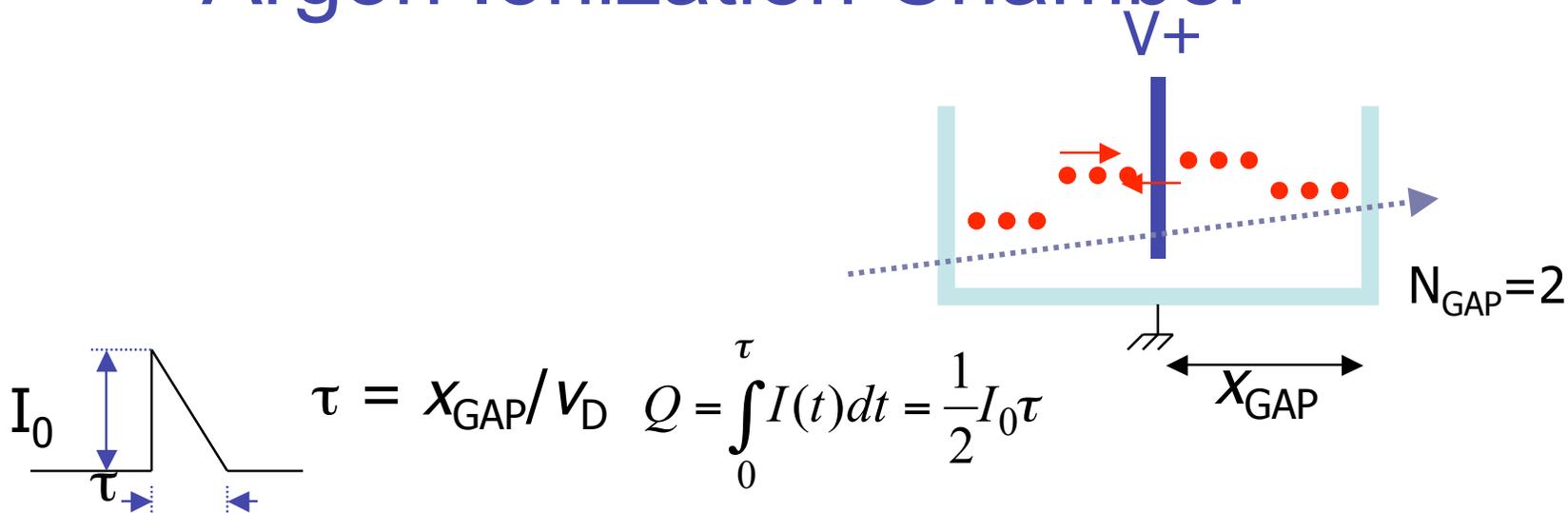


Installation and Integration in LHC

- After Sep.10 LHC conditions are now different
 - Tunnel access now much more limited
 - No early beam results
 - Extent of the shutdown and startup not yet known
 - Warmup and bakeout?
 - Uncertainty in LHC schedule
 - Will schedule our activities accordingly
- Detector installation
 - Two installed systems need retrofit + two additional systems ready to install
 - Will complete well in advance of 2009 startup as LHC access permits

LUMI - Conceptual Design

Argon Ionization Chamber



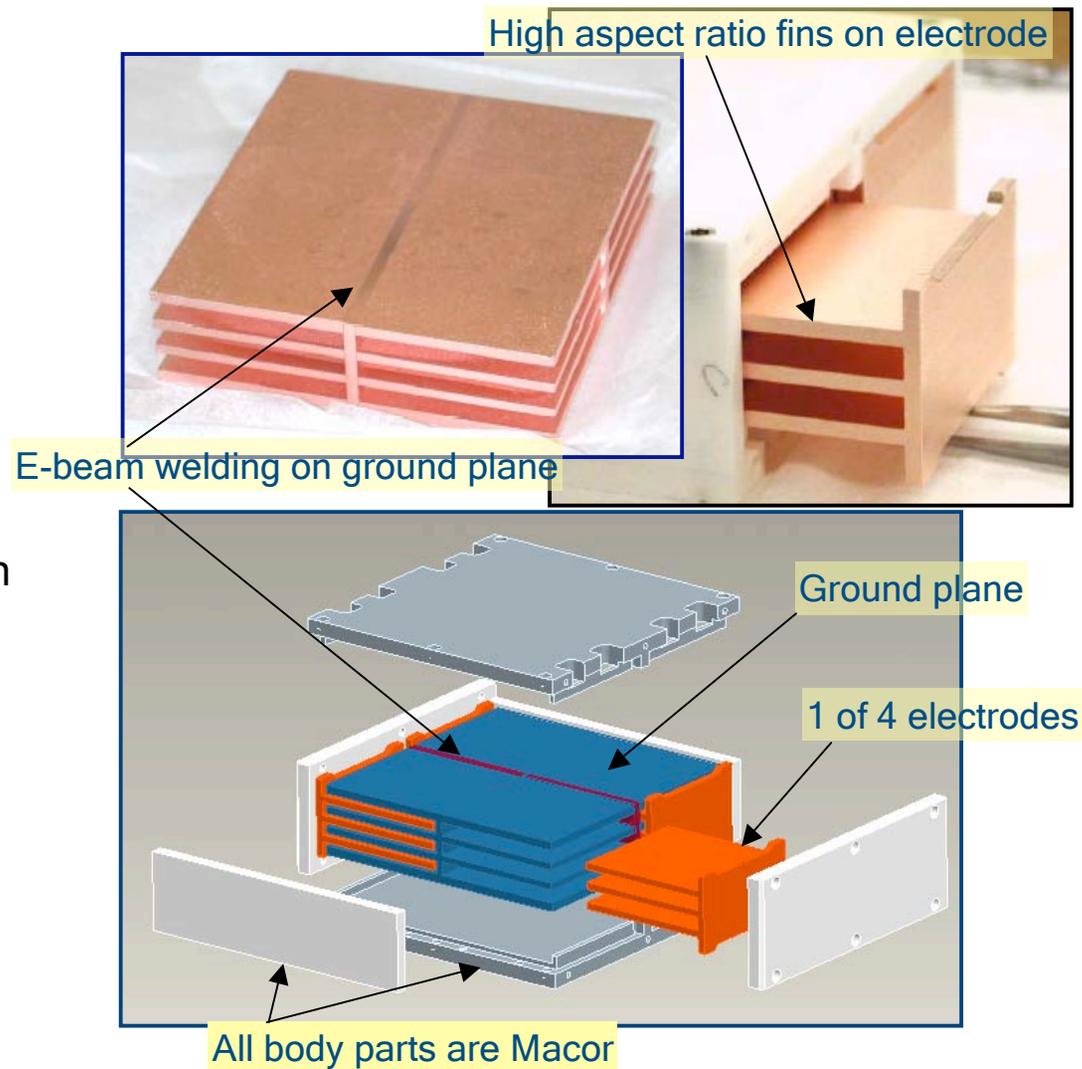
Signal is proportional to the number of parallel gaps
 Capacitance add up with n. of gaps + slows down the signal

→ Optimized for 6 gaps

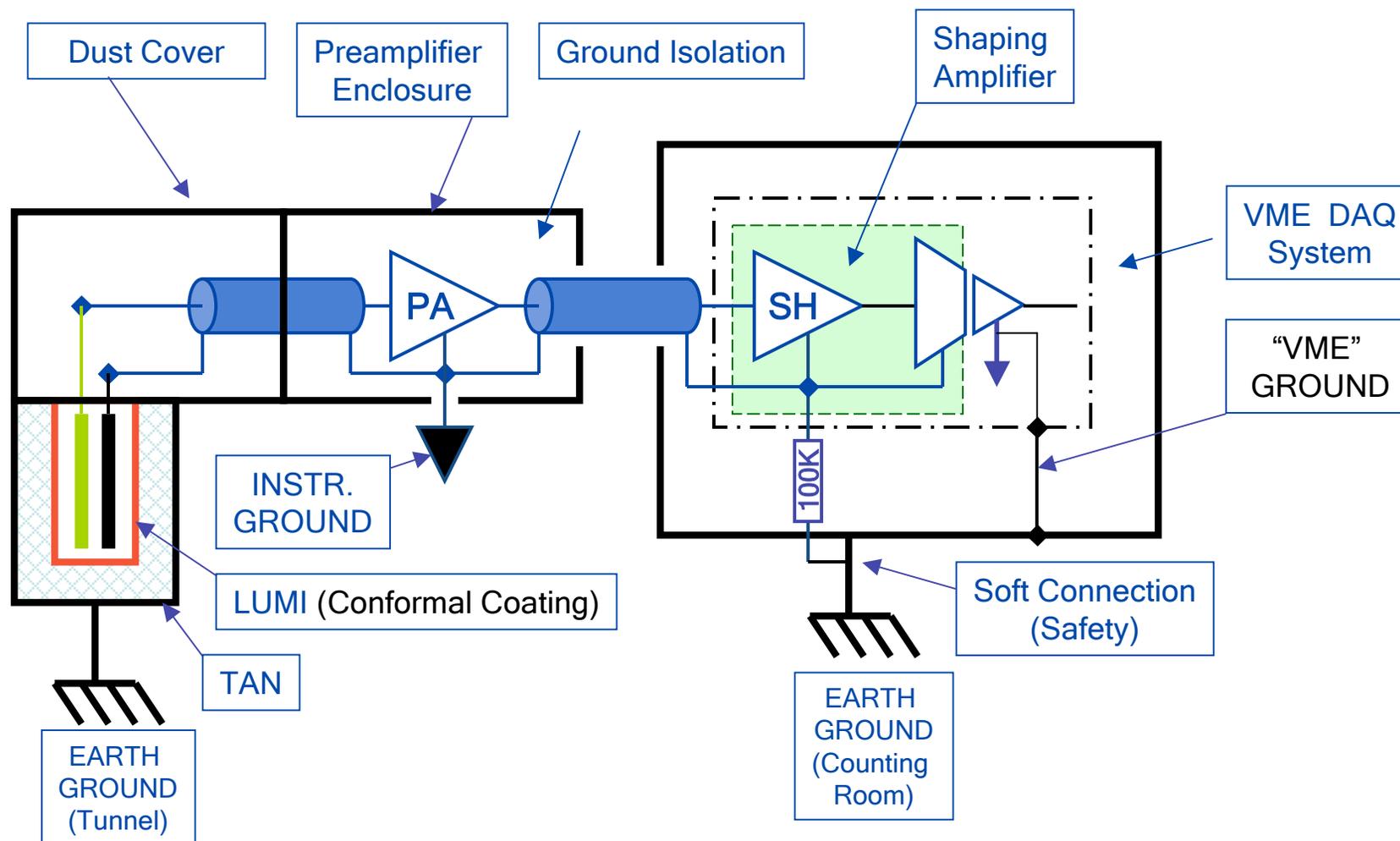
→ Must live in a radiation environment 100 x worse than
 accelerator instruments have ever seen

Ionization Chamber Fabrication

- Electrodes and ground plane
 - OFHC copper
 - Wire Electrical Discharge Machining (Wire-EDM)
 - High precision
 - Ground plane center element is e-beam welded
- Sensor body
 - Macor
 - Several fine features with high precision
 - Fasteners for assembly
 - Over-constrained assembly requires some craftsmanship



Electrical Connections

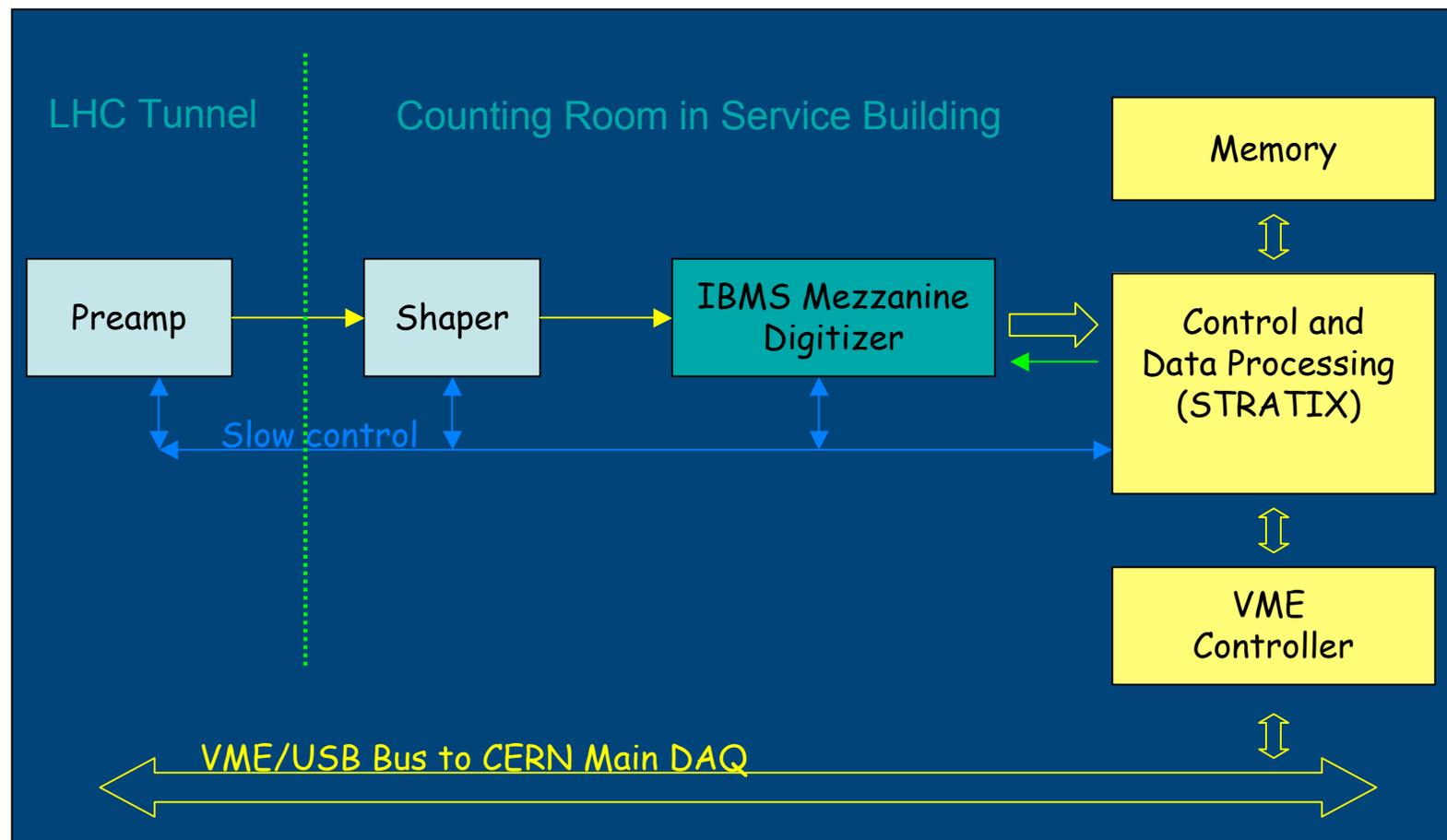




LUMI - Pulse Shaping + DAQ

- Active termination front end to properly compensate the chamber capacitance
 - Initial design in collaboration with Univ. di Pavia, INFN, Italy
- Pulse shaping electronics necessary to limit the noise bandwidth.
- Pulse shaping is also necessary to reduce the width of the pulse to accommodate the 40MHz repetition rate.
- Baseline recovery (Pole-Zero cancellation)
- Shaped pulse is digitized in a mezzanine board designed for the DABIV VME64 card used as standard interface by CERN - BI
- FPGA programming by LBL, controls programming by CERN

Signal Processing Path





Nomenclature

- Sensor - Copper/Macor assembly
- Detector - housing, steel pressure tank
- Pre-Amp Assembly
- Shaper - Chassis
- Detector Interface - Chassis



Progress Report

- Systems modeling and beam tests
- Detector fabrication
- Gas systems
- Preamps
- Readout systems
- Installation



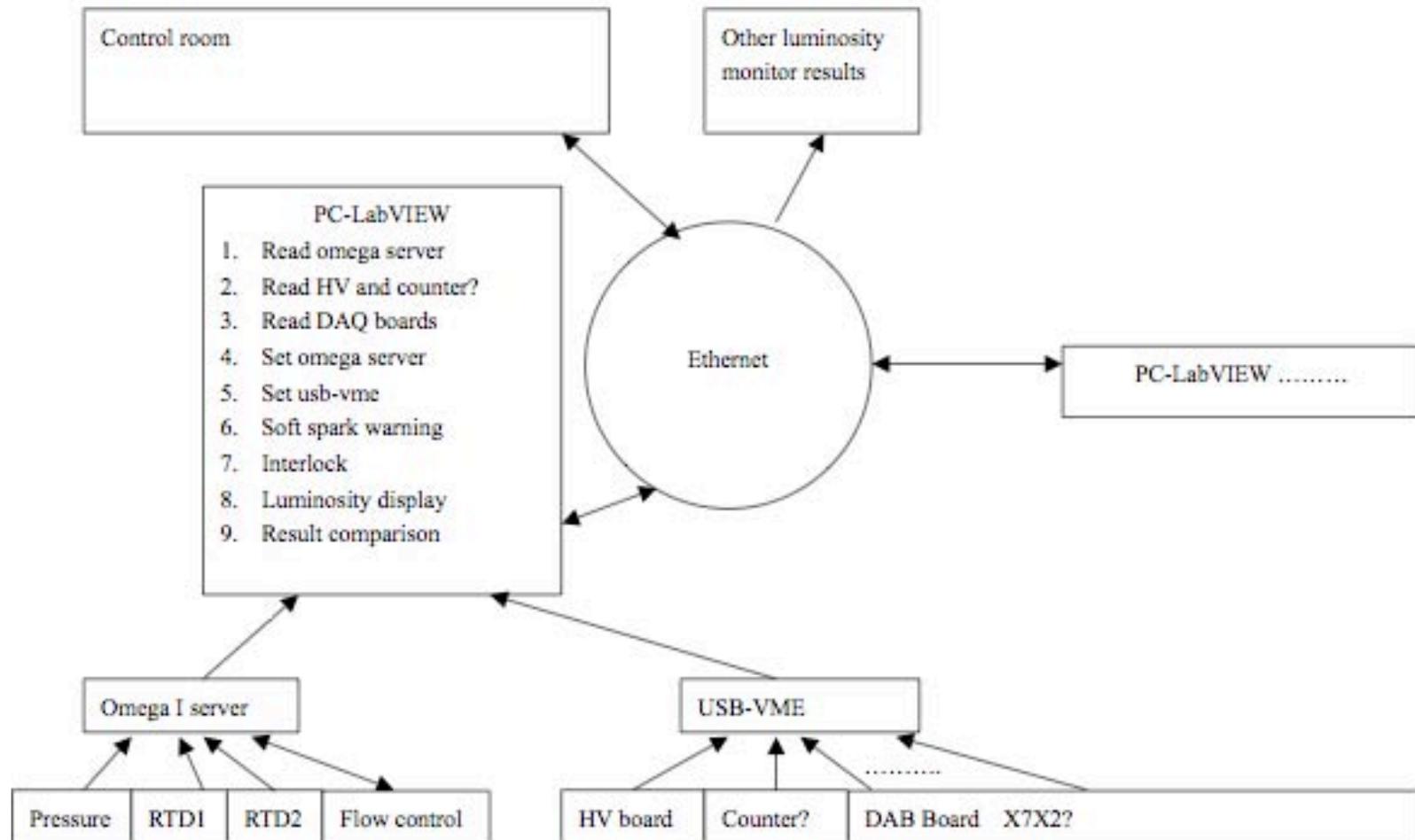
DAQ programming



DAQ Development

- Adopted firmware infrastructure from AB/BI group
 - Environment successfully imported at LBL
- Win/win for both groups
 - Much easier for CERN to import in FESA
 - LBL found most infrastructure work done
- Memory map defined
 - official interface between the LabView system from LBL and the LHC control system
- Effort included in LAFS
 - Help from Elliott McCrory (FNAL at CERN for LAFS) to integrate in the control system
 - AB/CO to deliver FESA class interface

DAQ System Layout





DAQ System Description and Status

- Defines parameters and functions
- Gas control panels and interlocks already developed
 - Need final hardware for testing

Omega read/write	USB-VME read/write	File write	Interlock logic
Read Pressure RTD1 RTD2	Read: HV board HV voltage ch1/2 HV current ch1/2 HV status ch1/2 DAQ board (X7X2) Stacking data Real time data	Data logger file Every 10s, 1file/hour? Avr/Max/Min for: Time stamp HV Voltage HV Current Gas pressure RTD1 RTD2 Histogram result 7X2X3564 channel	Spark rate ~ HV Gas pressure ~ HV
Write Iserver setup IDRX setupX3 Flow control?	Write HV board HV voltage ch1/2 HV Ramp ch1/2 HV current limit ch 1/2 DAQ board (X7X2) Threshold Line delay Counting interval Bunch filling pattern DSP filter coefficient Coincidence pattern Real time data ?	Spark diagnostic file All data for last ? ms Time stamp HV Voltage HV Current Gas pressure RTD1 RTD2 Real time data	Luminosity display AND Results comparison



DAQ Phased Development

FY08 - Phase I

- Programming environment
 - Crate operation and I/O
- Counting mode
- Stacking

FY09 - Phase II

- Pulse height mode
- Deconvolution
- Crossing angle



DAQ Interfaces

Top level memory organization

offset in words

0x0000 - 0x003f control and status registers

0x0040 - 0x0fff unused (wrapped version of first 32 words)

0x1000 - 0x3fff reserved

0x4000 - 0x4dec 4k averaged waveform

A0x5000 - 0x5dec 4k averaged waveform

B0x6000 - 0x6dec 4k counted waveform

A0x7000 - 0x7dec 4k counted waveform

B0x8000 - 0xffff reserved



DAQ Control Registers

Control and status registers	24
0 turn counter at start of acquisition	25
1 turns per buffer	26
2 Thresh A	27
3 Thresh B (in ADC unit, 0-4095, polarity in config reg)	28
4 DEADBEEF	29 turns lost
5 0	30 current value of turn counter
6 config register	31 status reg
7	
8-15 DSP configuration for ADC A	
16-23 DSP configuration for ADC B	



DAQ Status and Config Registers

Status Register - Bit

- 0 waveform buffer full
- 1 error flag (data lost, slow readout) read clear!!!!

Config Registers - Bit

- 0 discriminator polarity (0 above thres; 1 not above thres)
- 31-1 reserved



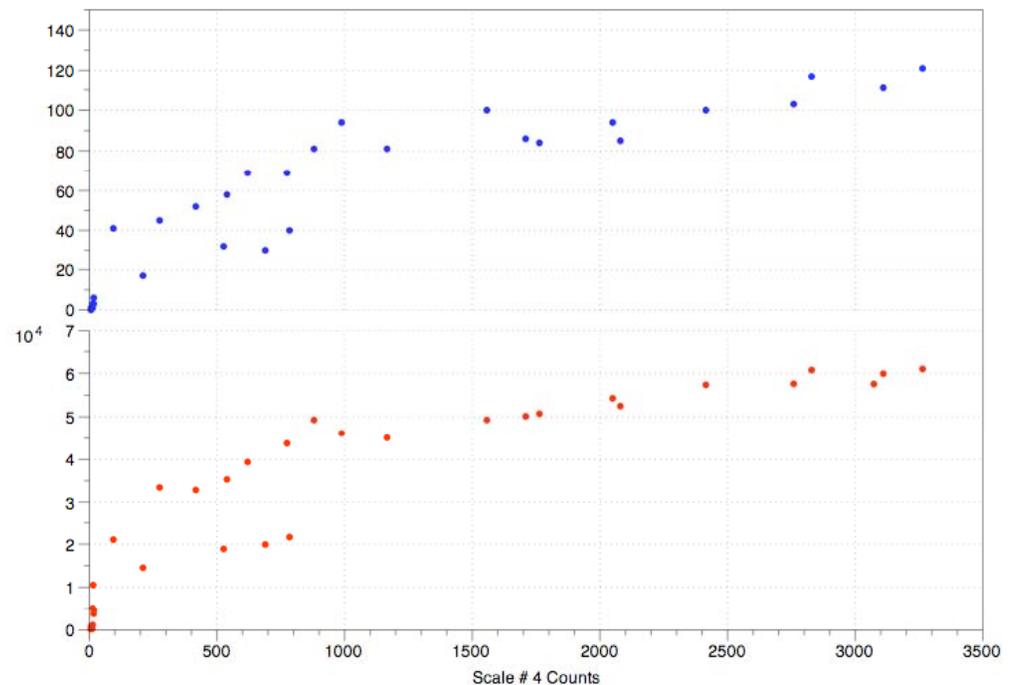
Double Buffer Feature

1. Poll 0x001f until the "1" bit is set (presumably we can raise an interrupt, so the driver doesn't waste cycles polling).
2. Read the data. If the next buffer completes before this one is "unloaded" (see the following step), data (whole turns) will be dropped rather than corrupt the readout in progress. That turn-dropping behavior will lead to a set "2" bit in 0x001f.
3. Read 0x0000 through 0x001f to determine the conditions that apply to the data. The act of reading the last location(0x001f) marks the buffer just read as "unloaded".
4. When the next buffer is full, the firmware will flip acquisition to the "unloaded" buffer, and set the 0x001f"1" bit, allowing the process to repeat.



Test during SPS beam test

- First test in the SPS
 - Good agreement with NIM scalers
 - Some adjustment required
- Learned we need an even/odd gain and offset adjustment
 - IBMS boards have two digitizers each





Systems Integration

Test all parts and components

Integration impacts signals and HV performance

Supporting Electronics

Racks are ready in both counting rooms

- CERN installed:
 - VME crates
 - BOBR board for orbit clock
 - Network hub
 - Cable patch panels for semi-rigid cables
 - DC ps for shapers
- LBL adding:
 - Boards and modules
 - Local readout points
 - Distribution system to share signals

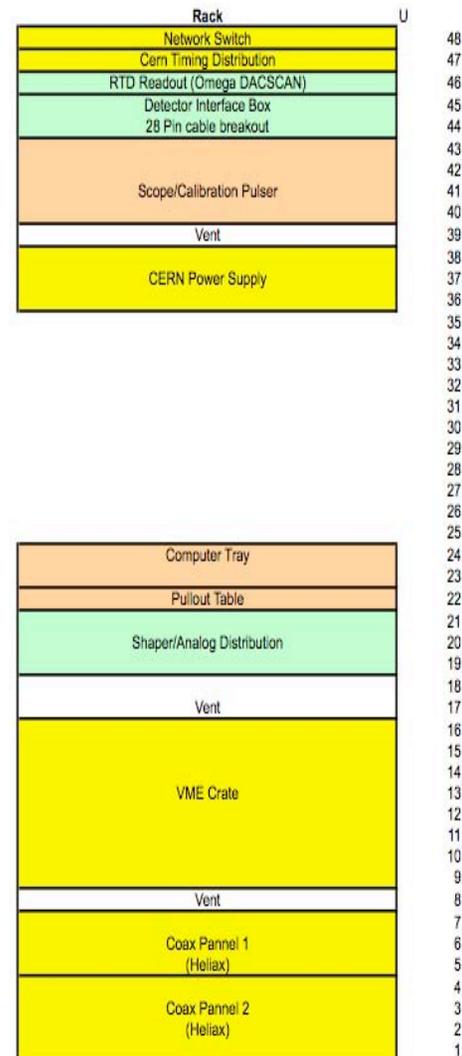


IP1 Rack



Racks Layout

- CERN provided (Yellow)
- LBL Provided (Green)
- Purchases - by LBL (Tan)

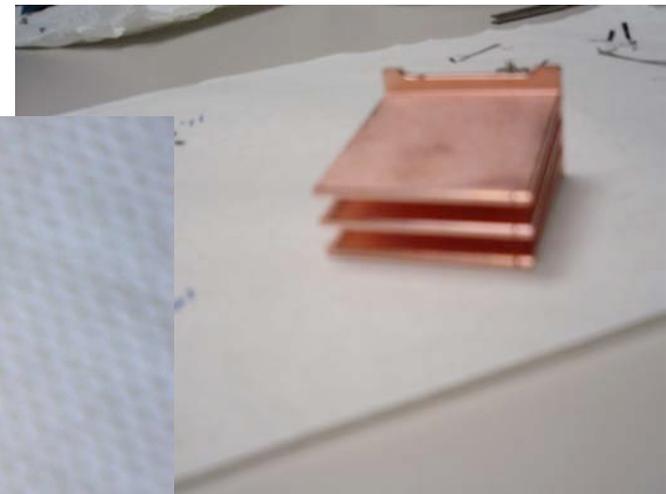




Gas Systems

- Designed, built, installed, tested
- Software commissioning underway
- Described by Howard next

Sensor Assembly - 1



Comb Enhanced
by LBL shop



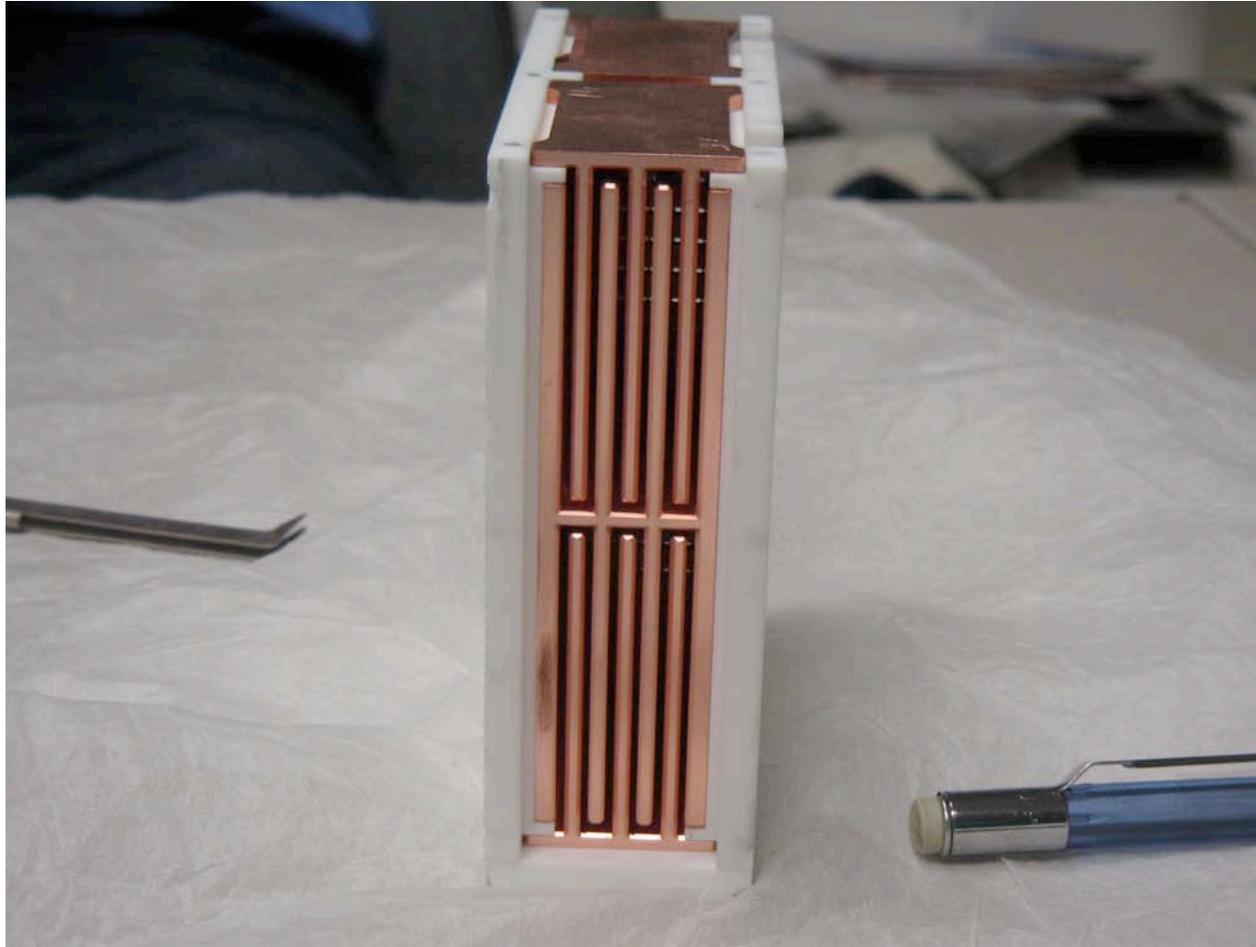
Sensor Assembly - 2

- Mount ground block to ceramic
- Connect lower quadrants
 - Carefully shim to fit and align
- Connect upper quadrants
 - Shim as above
- Close ceramic housing
 - Pay attention to gas path
 - Make sure block mount holes are properly mounted
- Assembly takes ~ 6 - 8 hours

Note chamfer on detector edges to reduce peak fields

Added after HV problems in testing

Sensor Assembly - 3





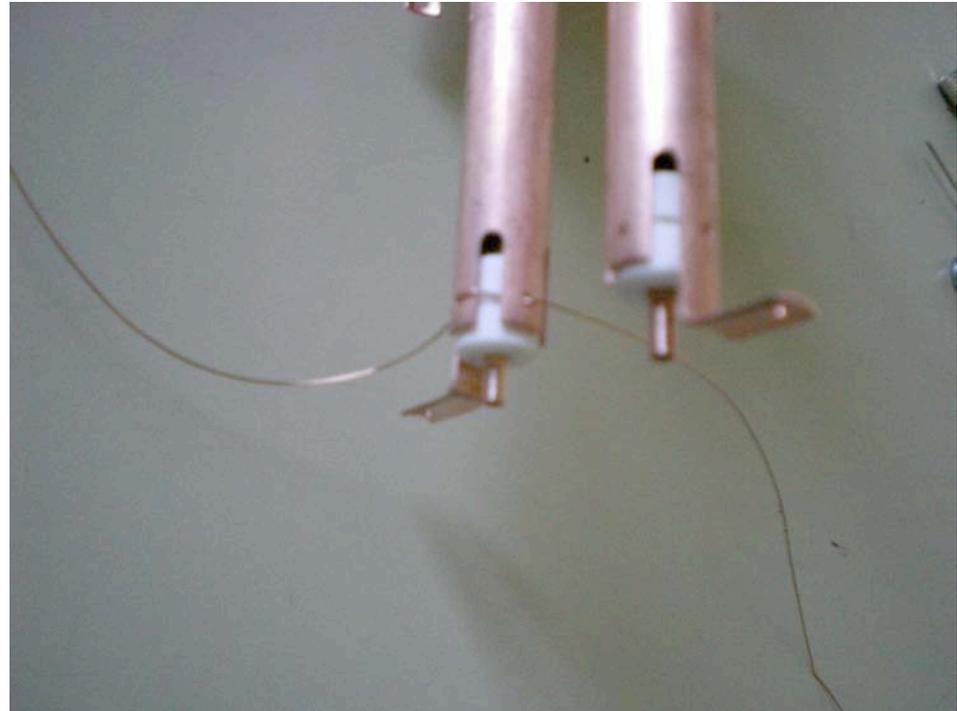
Detector Assembly

- Install glass + ceramic insulators
- Install safety wire
- Mount copper block
 - Should be able to avoid this step in the retrofit
- Mount Detector to support block
- Connect quadrants
- Connect RTDs

TEST

Detector Assembly - 1

1. Install inner conductors, glass and ceramic insulators
2. Safety wiring holds ceramic stops

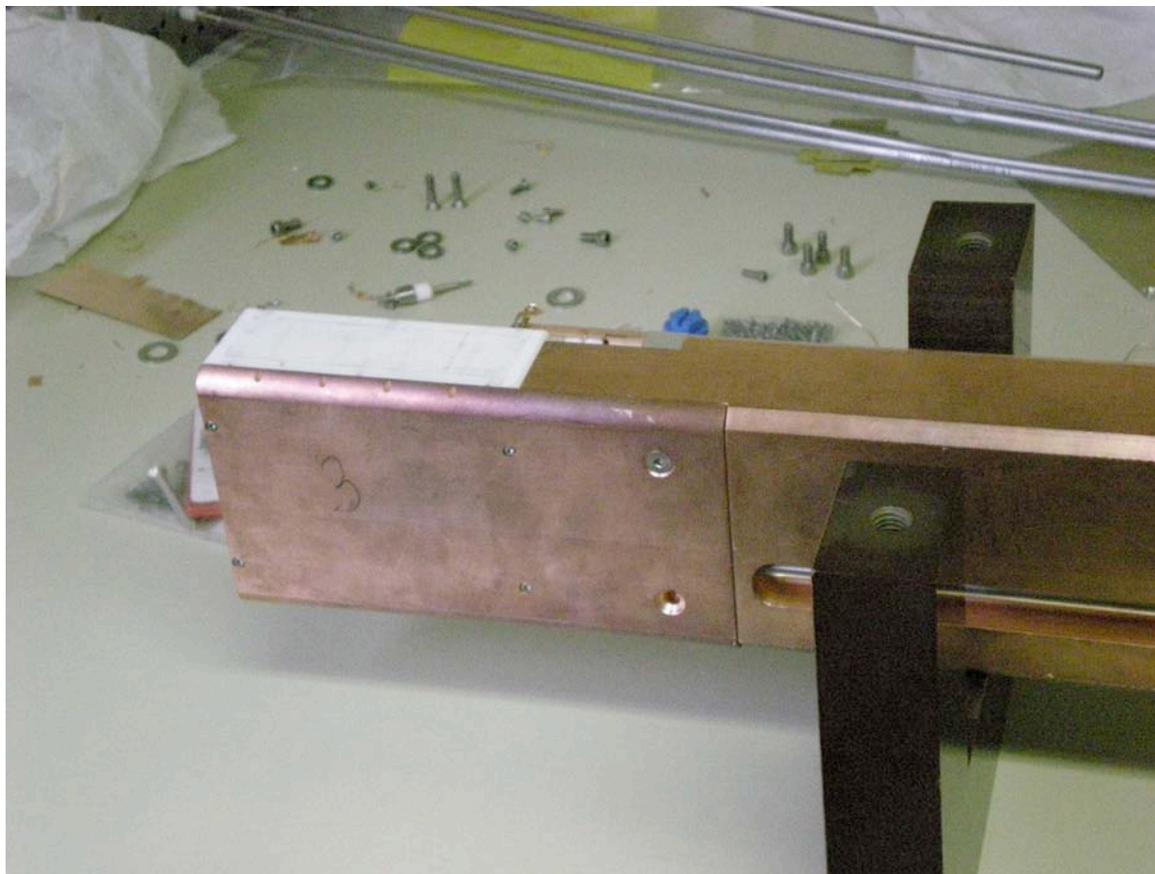


Detector Assembly - 2

3. Mount copper support block to flange

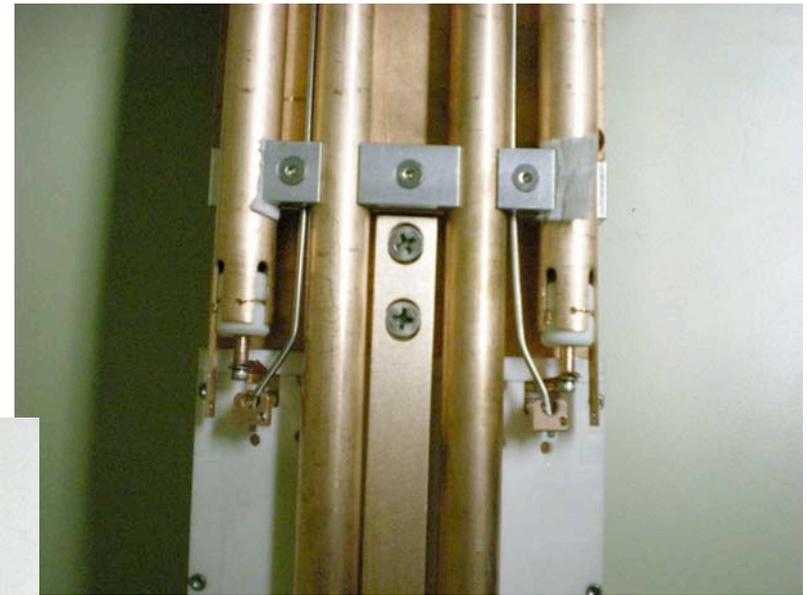
Gas feedline connected

4. Mount sensor assembly on copper support block



Detector Assembly - 3

5. Custom made connections to each quadrant



Adjusted for HV
performance

Detector Assembly - 4



Install on housing
TiN seal

Conclusions

- Significant progress in all aspects of the project
- Observed beam on day one with one detector
 - Ready with a second one 5 days later
- Delivered gas systems, DAQ and software readout
- All detectors at CERN
 - Installation planning started
- Underway with system integration
- Beam test results prove detector performance